LTCC as MCM Substrate: Design of Strip-Line Structures and Flip-Chip Interconnects

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***Abstract* — LTCC multilayer substrates offer a cost-effective MCM solution for frequencies around 20 GHz and beyond. This paper reports on LTCC-specific transmission-line structures using a commercially available process. For the chip interconnect, a flip-chip approach contacting the backside is chosen, which, in a first step, is realized on conventional ceramics.**

I. Motivation

Cost-effective approaches for multi-chip modules are a prerequisite for systems in the emerging wireless and satellite communication markets beyond 20 GHz. Low-temperature cofired ceramics (LTCC) offer an a promising solution in this regard since they combine low-cost processing with flexibility in terms of multilayer wiring. One has to pay for this, however, by larger line sizes and tolerances compared to the conventional ceramics processes.

Recently, work on LTCC structures in the 24 GHz range [1] and a 30 GHz drop-on filter [2] was published, which highlighted the potential of this approach. Based on an in-house LTCC glass-ceramics technique, even a 77 GHz package has been demonstrated [3]. Moreover, including a metal base (LTCC-M) opens new possibilities in reducing shrinkage and improving heat sinking (see [4]). This outlines that dimensional tolerances are still an issue in high-frequency applications, particularly when relying on the openly available LTCC processes, which were developed for much lower frequencies.

Within this framework, our paper reports on work that is to investigate what can be achieved when using a commercially available LTCC process. The emphasis is on the following two issues:

(i) To investigate LTCC-typical transmission-line structures, e.g. the buried strip line, together with the basic transition elements.

(ii) To adopt the flip-chip concept to LTCC by using a chip-up approach similar to [5], which is compatible with microstrip chip-design and eliminates detuning problems.

The design and measurements results related to item (i) are presented in Sec. II. Regarding the flip-chip part, in a first step the chip-up version is treated in conjunction with a conventional ceramic motherboard. An optimized flip-chip interconnect was designed. Presently, the test chips are in fabrication.

II. LTCC Transmission-Line Structures

Basically, one has to distinguish between the lines located at the top or bottom surface of a multi-layer board and the buried ones, which involve only inner layers. Regarding the first group, mainly microstrip (MS) or coplanar waveguide (CPW) are of interest. Within the LTCC structure, strip lines (SL) represent an advantageous choice because dispersion and radiation are negligible and upper and lower ground metalizations provide shielding and may be used as ground for other lines. Therefore, in the approach described here we use two line types: microstrip at the surfaces and strip-line within the LTCC board. This allows surface mounting of chips etc. as well as realization of crossings.

Applying this concept requires one elementary transition element: the microstrip-to-strip-line transition connecting the microstrip on the surface to the buried strip-line.

In the following, we briefly discuss microstrip and strip line and then treat the MS-to-SL transition in more detail.

A. Microstrip and StripLines

Microstrip and strip-line geometry depend on restrictions related to the LTCC technology. This is, on the one hand, the necessity that the layer thickness is an integer multiple of a single LTCC ceramic layer, which is determined by the process. On the other hand, the design rules regarding metalization and the dimensional tolerances need to be accounted for.

In accordance with the manufacturer's specifications we chose 3 ceramic layers for the microstrip (resulting in a total substrate thickness of about 250 µm) and 3 + 3 ceramic layers for the strip line. This yields reasonably sized strip widths for 50 Ω lines and allows also to choose higher impedances up to 70 Ω without design-rule violation.

Measurements of the homogeneous microstrip line connected to two prober pads show good agreement in phase

constant and a slightly deviating characteristic impedance of 52 Ω, which can be explained by the process tolerances. Only attenuation is higher than predicted, the reasons of which are presently under investigation.

B. Microstrip-to-strip-line Transition

To connect the surface-bound microstrip line to the buried strip line the 5-via transition structure depicted in Fig. 1 was developed. Four of the vias connect the ground metalizations of strip line and microstrip providing also shielding of the transition. The center via connects the signal lines. An essential feature of this structure is that it can be extended easily to the case, where additional ceramics layers are inserted between the microstrip ground and the upper strip-line ground or where microstrip and strip line form a 90° bend. Thus it forms the elementary transition element for multi-layer wiring.

Design goal for the transition was a reflection below -26 dB in the frequency range 17...22 GHz. To achieve this, several layout variants had to be considered, followed by optimizations. All this design work was performed by means of electromagnetic simulation. For this purpose, our in-house finite-difference frequency-domain software was employed (for the method, see, e.g., [6]).

In the optimization process, mainly the diameter of the hole through the microstrip ground, which at the same time is the upper strip-line ground, and the distance of the four ground vias were varied.

After optimization of these parameters we found that the transition overall had still a large capacitive effect, caused to a significant part by the lower ground of the strip line in the transition region. To reduce the parasitic influence of this part while preserving shielding the arrangement in Fig. 1 was chosen, where the critical ground part is moved down two layers beneath the lower ground of the strip line. In this way, the specifications could be met.

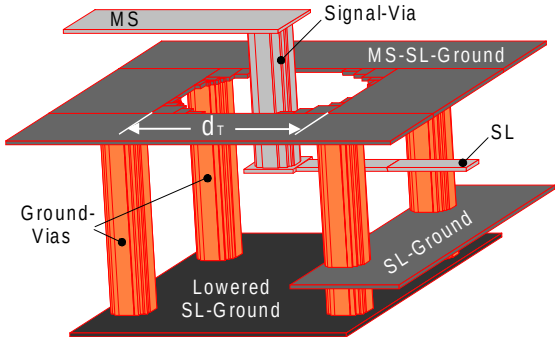

Fig. 1. The MS-to-SL-transition (LTCC layers not shown).

Furthermore, in order to increase the margin, the small remaining capacitive load is compensated by a short inductive line section between signal via and strip line (see Fig. 1).

In order to verify the properties of the optimized transition, the back-to-back structure illustrated by Fig. 3 was fabricated and measured. The total length is 14 mm, the section of the buried strip line is 8.35 mm between the centers of the two signal vias. Also, a second version with 23.6 mm total length and a 17.95 mm SL section was fabricated.

Design validation is a difficult task since the transition can be probed only in a complex environment involving

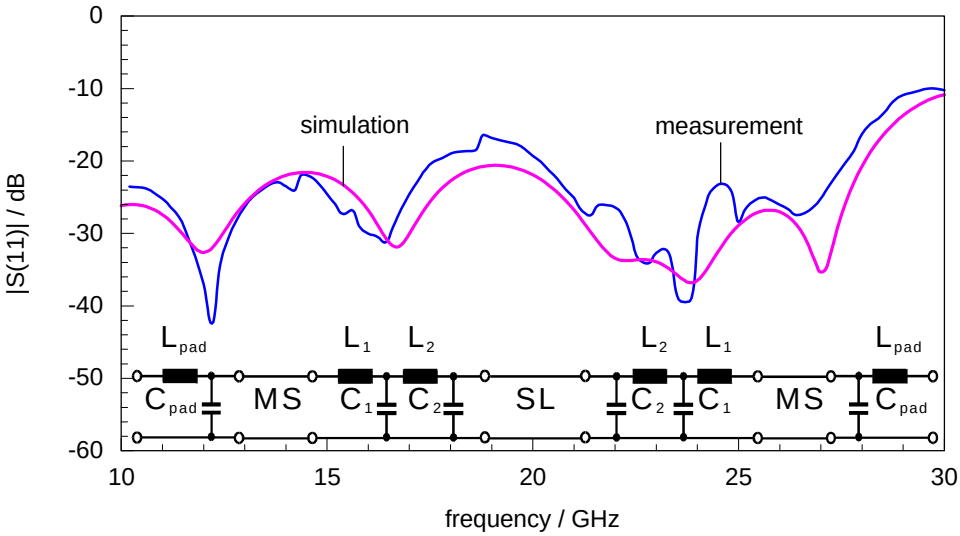

Fig. 2. Measured and simulated reflection of the back-to-back structure in Fig. 3 with two MS-to-SL-transitions; the inset shows the equivalent-circuit model consisting of the prober-pads, the MS-to-SL transitions (L_1, L_2, C_1, C_2) and the MS and SL sections.

prober pads and MS and SL line sections. Therefore, additional reference structures were realized on the same LTCC carrier. They are used to extract the equivalent circuit of the pads and to determine the microstrip line parameters. The inset in Fig. 2 shows the equivalent-circuit description of the test structure in Fig. 3. The elements L_1, L_2, C_1, and C_2 represent the MS-to-SL transitions and are determined by the electromagnetic simulations.

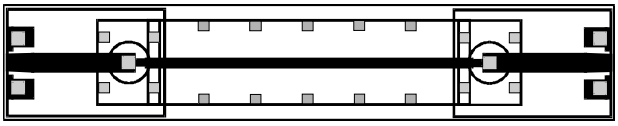

Fig. 3. Layout of the MS-SL-MS test structure with pads for on-wafer probing (total length is 14 mm, distance between vias 8.35 mm).

Fig. 2 presents measured and modeled reflection data for the test structure. The results show good agreement, even in the range below -20 dB. Already small changes (+/- 3%) of the values for L_1 and C_1 cause considerable deviations in S_{11}. This high sensitivity together with the low S_{11} values in Fig. 2 verifies that the transition exhibits the desired high return loss.

At a first glance, one would expect an overall S_{11} below -20 dB in the target range around 20 GHz. The measurements exceed this limit slightly. Further investigations show that this is due to an impedance mismatch of the MS and the SL. Taking into account the reference structures, one finds that the actual MS characteristic impedance is 52 Ω, that of the SL 53 Ω. This points out importance of the tolerance issue, which is an essential limitation of the LTCC processes: Even if a transition reaches 30 dB return loss, this value will not be effective since impedance variation of the homogeneous line sections due to dimensional tolerances will superimpose and limit minimum reflection.

III. The Modified Flip-Chip Interconnect

The conventional flip-chip interconnects offer excellent performance up to mm-wave frequencies if bumps with diameters in the 30 µm range are used [7]. Even with larger bumps (80 µm diameter) low reflection can be achieved by means of compensation [8]. Nevertheless, unwanted effects, such as detuning of the circuit on the chip, the problem of optical inspection of the mounted chips, the limited heat-transfer capability, and the lack of compatibility with microstrip chips make flipped chips less attractive. These disadvantages can be avoided by using face-up mounted chips as illustrated in Fig. 4 (a), which is referred to as "hot-via" configuration in the following.

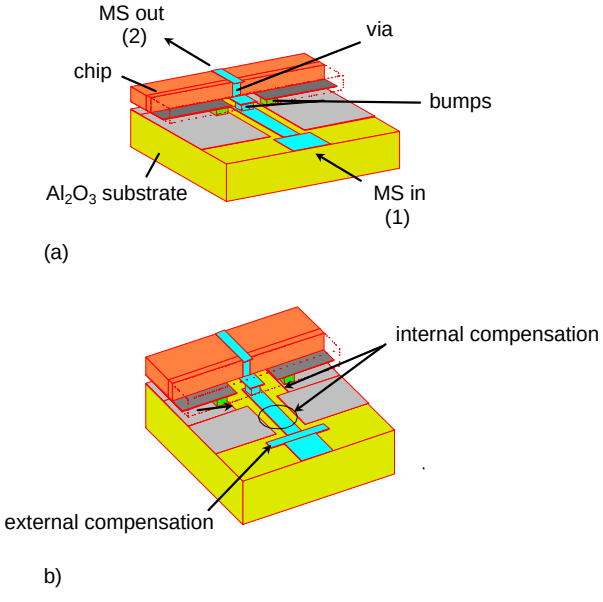

Fig. 4 "Hot-via" transition without (a) and with (b) compensation (chips are mounted face-up, signal path from motherboard is through bump and via to the chip, chip substrate partly blanked to show via).

The microstrip signal line is connected to a backside pad by a via-hole. The interconnect to the motherboard is then performed by common flip-chip bumps. On the carrier substrate, a transition to microstrip follows. The question is whether this hot-via interconnect can compete with the conventional flip-chip scheme in the frequency range up to about 40 GHz. In order to clarify this, electromagnetic simulations using our 3D finite-difference frequency-domain code [6] were performed.

Fig. 4 (a) shows the basic structure under investigation. Bumps with a diameter of 80 µm and 50 µm height are assumed. Fig. 5 presents the simulation results. For the uncompensated case, one finds that the -20 dB level is reached already at 18 GHz. However, this provides enough margin for improvement when using appropriate compensation techniques. The magnitudes of S_{11} and S_{22} do not agree fully due to the existence of unwanted modes in the chip area, which are excited weakly. Further investigations reveal that the capacitive behavior of the interconnect dominates due to the overlap of chip and motherboard.

In order to improve the interconnect performance with regard to broad-band 38 GHz applications, compensation measures were added as illustrated by Fig. 4 (b). High impedance coplanar-line sections are introduced within the interconnect area. In order not to waste expensive chip

area, the backside of the chip is designed with special care. For fine-tuning, an additional section is inserted in the microstrip line on the carrier substrate.

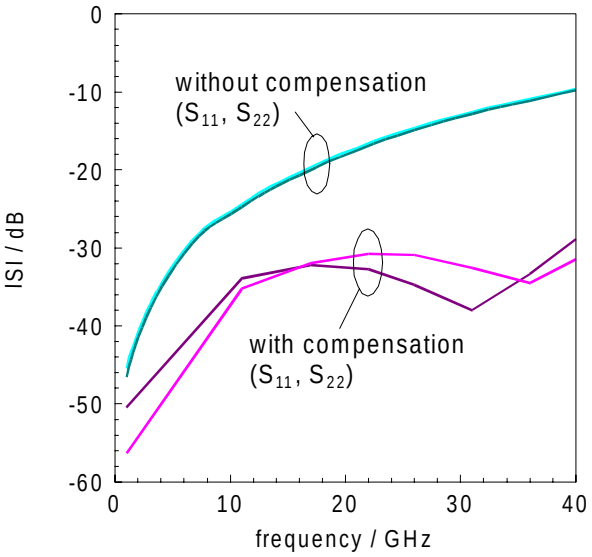

Fig. 5. Simulated reflection coefficient of the hot-via single transition with and without compensation as a function of frequency (bump geometry: height 50 µm, diameter 80 µm).

As can be seen from Fig. 5, the compensated hot-via transition exhibits the desired characteristics: reflection remains well below -20 dB up to 40 GHz. These results demonstrate that the hot-via scheme may be successfully used in this frequency range. In order to validate the simulation data fabrication of test structures is presently in progress. After verification of the basic concept investigations will be performed to replace the alumina substrate by an LTCC multi-layer.

IV. Conclusions

A transmission-line concept for multi-layer LTCC substrates is presented taking into account restrictions of a commercially available LTCC process. It consists of microstrip and buried strip line together with an optimized and versatile elementary transition, which reaches a return loss level above 20 dB up to frequencies of 28 GHz. At higher frequencies, particularly process tolerances become a critical limitation.

For chip mounting on the LTCC motherboard, the so-called hot-via approach is chosen, which is similar to the conventional flip-chip scheme, but with microstrip chips mounted face-up. In a first step, in order to verify properties of this new approach, a conventional ceramic substrate is used as motherboard. An optimized interconnect design was developed by means of em simulation, which achieves return losses above 20 dB broad-band up to 40 GHz. The corresponding test structures are presently in the fabrication. The simulation data indicate that this type of interconnect may be applied up to the 40 GHz frequency range.

Acknowledgement

This work has partially been funded by the European Space Agency.

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